Amendments to the Claims:

A clean version of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121(c). This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-5. (Cancelled).

6.- 23. (Cancelled)

24. (Currently Amended) A MOS transistor, comprising:

a semiconductor substrate having a top surface;

isolation regions formed in said substrate;

a gate structure formed over said substrate having sidewalls disposed on ~~either~~both sides of said gate structure;

a source region having a source lightly doped region and a source heavily doped ~~drain~~ region, wherein an impurity concentration of said source lightly doped region is lower than an impurity concentration of said source heavily doped region, each of which having an upper portion in contact with the side wall, wherein the source lightly doped region is formed below one of said sidewalls and said impurity concentration decreases as a depth from the top surface of the substrate increases, said source heavily doped region being disposed between said source lightly doped region and said isolation region, and wherein a portion of said source lightly doped region extends

beneath a gate oxide of said gate structure;

a drain region having a drain lightly doped region and a drain heavily doped region, wherein an impurity concentration of said drain lightly doped region is lower than an impurity concentration of said drain heavily doped region, wherein the drain lightly doped region is formed below one of said sidewalls, wherein said drain heavily doped ~~drain~~ region is disposed between said drain lightly doped region and said isolation region and wherein a portion of said drain lightly doped region extends beneath a gate oxide of said gate structure; and

metallic silicide layers respectively formed on said source heavily doped regions and said drain heavily doped regions, said metallic silicide layers being in contact with said sidewalls and said isolation regions, and extending onto said isolation regions, wherein undersides of said metallic silicide layers are substantially coplanar with respective undersides of said sidewalls in contact with said top surface.

25. (Previously Presented) A MOS transistor as recited in claim 24, wherein said metal silicide layers are formed between each of said sidewalls and said isolation regions.

26. (Previously Presented) The MOS transistor according to Claim 25, wherein said metal silicide layers have undergone implantation of an impurity by an ion implantation method prior to said thermal diffusion of said impurity and wherein said side walls are composed of insulating materials which has undergone implantation of an impurity by said ion implantation method prior to said thermal diffusion of said impurity from said side walls.

27. (Previously Presented) The MOS transistor according to Claim 24, wherein an impurity concentration in said source lightly doped region is almost the same as that in said source heavily doped region.

28. (Previously Presented) The MOS transistor according to Claim 24, wherein an impurity concentration in said source lightly doped region is substantially smaller than that in said source heavily doped region.

29. (Previously Presented) The MOS transistor according to Claim 24, wherein an impurity concentration in said drain lightly doped region is almost the same as that in said drain heavily doped region.

30. (Previously Presented) The MOS transistor according to Claim 24, wherein an impurity concentration in said drain lightly doped region is substantially smaller than that in said drain heavily doped region.

31. (Previously Presented) The MOS transistor according to Claim 24, wherein each of said side walls extends on said semiconductor substrate in a direction in which both said side walls are brought near to each other from side portions of both said electrodes facing each other and wherein a gate electrode is formed in a manner that its both sides are disposed on said side walls.

32. (Currently Amended) A semiconductor device, comprising:
a semiconductor substrate having a top surface;

isolation regions formed in said substrate, and which define active regions;

MOS transistors respectively disposed in said active regions, each of said MOS transistors having a gate structure, a source region, a drain region and sidewalls disposed on either side of each of said gate structures;

wherein each of said source regions has a source lightly doped region and a source heavily doped ~~drain~~ region, each of which having an upper portion in contact with the side wall, wherein an impurity concentration of said source lightly doped region is lower than an impurity concentration of said source heavily doped region sidewalls and said impurity concentration decreases as a depth from the top surface of the substrate increases, wherein the source lightly doped region is formed below one of said sidewalls, and wherein said source heavily doped region is disposed between said source lightly doped region and one of said isolation regions;

wherein each of said drain regions has a drain lightly doped region and a drain heavily doped region, wherein an impurity concentration of said drain lightly doped region is lower than an impurity concentration of said drain heavily doped region, wherein the drain lightly doped region is formed below another of said sidewalls, and wherein said drain heavily doped ~~drain~~ region is disposed between said drain lightly doped region and said isolation region; and

metallic silicide layers respectively formed on said source heavily doped regions and said drain heavily doped regions, said metallic silicide layers being in contact with said sidewalls and said isolation regions, wherein undersides of said metallic silicide layers are substantially coplanar with respective undersides of said sidewalls in contact with

said top surface.

33. (Previously Presented) A semiconductor device as recited in claim 32, wherein said metal silicide layers are formed between each of said sidewalls and said isolation regions.

34. (Previously Presented) The semiconductor device according to Claim 32, wherein said metal silicide layers have undergone implantation of an impurity by an ion implantation method prior to said thermal diffusion of said impurity and wherein said side walls are composed of insulating materials which has undergone implantation of an impurity by said ion implantation method prior to said thermal diffusion of said impurity from said side walls.

35. (Previously Presented) The semiconductor device according to Claim 32, wherein an impurity concentration in said source lightly doped regions is almost the same as that in said source heavily doped regions.

36. (Previously Presented) The semiconductor device according to Claim 32, wherein an impurity concentration in said source lightly doped regions is substantially smaller than that in said source heavily doped regions.

37. (Previously Presented) The semiconductor device according to Claim 32, wherein an impurity concentration in said drain lightly doped regions is almost the same as that in said drain heavily doped regions.

38. (Previously Presented) The semiconductor device according

to Claim 32, wherein an impurity concentration in said drain lightly doped regions is substantially smaller than that in said drain heavily doped regions.

39. (Currently Amended) The semiconductor device according to Claim 32, wherein each of said side walls extends on said semiconductor substrate in a direction in which both said side walls are brought near to each other from side portions of both said electrodes facing each other and wherein a gate electrode is formed in a manner that its both sides are disposed on said side walls.